29th IEEE Workshop on Signal and Power Integrity

May 11-14, 2025 – Gaeta, Italy

WORKSHOP PROGRAM

May 11, Sunday	
14:20-14:50	Registration
14:50-15:00	**Tutorials Welcome**
15:00-16:00	**TUTORIAL** **Grégory Houzet**
16:00-16:30	*Coffee-Break*
16:30-17:30	**TUTORIAL** **Marco Donald Migliore**
18:30 onwards	**Welcome Reception**

May 12, Monday	
08:30-09:00	Registration
09:00-09:20	**Opening Session**
09:20-10:00	**KEYNOTE** **Wendem Beyene**
10:00-10:40	**SESSION 1.1** **AI-Based Methods and Models**
10:40-11:10	*Coffee-Break*
11:10-12:30	**SESSION 1.2** **AI-Based Methods and Models**
12:30-14:00	*Lunch*
14:00-14:40	**KEYNOTE** **Giovanni Frattini**
14:40-15:40	**SESSION 2** **Design Optimization**
15:40-15:50	Activity IEEE TC-EDMS
15:50-16:00	Sponsor Pitch **STMicroelectronics**
16:00-16:40	**POSTER SESSION** *& Coffee-Break*
17:30 onwards	**City Tour**

May 13, Tuesday	
09:00-10:20	**SESSION 3** **Macromodeling**
10:20-10:30	Sponsor Pitch **Huawei**
10:30-10:40	Sponsor Pitch **ESSS-Ansys**
10:40-11:00	*Coffee-Break*
11:00-12:30	**INDUSTRY PANEL**
12:30-14:00	*Lunch*
14:00-14:40	**KEYNOTE** **Andrea Ferrari**
14:40-15:40	**SESSION 4** **High Speed Channels**
15:40-16:00	*Coffee-Break*
16:00-17:00	**SESSION 5** **Measurement Based Models**
18:30 onwards	**Gala Dinner**

May 14, Wednesday	
09:00-10:20	**SESSION 6** **Package Design / Power Integrity**
10:20-10:50	*Coffee-Break*
10:50-12:10	**SESSION 7** **Cross Talk & Noise Reduction / Memristors**
12:10-12:30	**Closing Session**
12:30-14:00	*Lunch*
14:00-18:00	**IBIS Summit**

WORKSHOP PROGRAM

TUTORIALS AND TECHNICAL SESSIONS

May 11, Sunday

14:50 – 15:00 **TUTORIALS WELCOME**

15:00 – 16:00 **TUTORIAL**

Grégory Houzet
Université Savoie Mont Blanc, France
High Frequency Measurements, Parameters Extraction Techniques and Microelectronic Materials Characterization

16:30 – 17:30 **TUTORIAL**

Marco Donald Migliore
University of Cassino and Southern Lazio, Italy
S-parameter Measurement and Calibration Techniques

May 12, Monday

09:00 – 09:20 **OPENING SESSION**

09:20 – 10:00 **KEYNOTE**

Wendem Beyene
Reality Labs, Meta Platforms, USA
The Challenges in Signal Integrity and Power Integrity to Meet the Demands of Expanding and Evolving Compute Platforms

SESSION 1.1
10:00 – 10:40 **AI-BASED METHODS AND MODELS**
Chair: Mihai Telescu

10:00
Jose Enrique Hernandez-Bonilla (1), Torben Wendt (1), Torsten Reuschel (2), Cheng Yang (3), Christian Schuster (3)
(1) Robert Bosch GmbH, Germany; (2) University of New Brunswick, Canada; (3) Technische Universität Hamburg, Germany
Data-Driven Prediction of Temperature-Dependent Dielectric and Conductive Parameters Based On Differential Stripline Characteristics

10:20
Devi Sreekumar, Shalabh Gupta
Indian Institute of Technology Bombay, India
Efficient Synthesis and Simulation of High-Density Interconnects using Machine Learning

SESSION 1.2
11:10 – 12:30 **AI-BASED METHODS AND MODELS**
Chair: Tom Dhaene

11:10
Marco Atlante (1), Riccardo Trinchero (1), Igor S. Stievano (1), Mihai Telescu (2), Noël Tanguy (2)
(1) Politecnico di Torino, Italy; (2) Univ. Brest, Lab-STICC, CNRS, France
SPICE-based Behavioral Models of IC Buffers via Compact Kernel Regressions

11:30
Michele Cusano (1), Riccardo Trinchero (1), Igor S. Stievano (1), Stefano Grivet-Talocia (1), Paolo Manfredi (1), Stefanie Schatt (2)
(1) Politecnico di Torino, Italy; (2) Continental Automotive Technologies GmbH, Germany
A Multi-Output Active Learning Method for the Uncertainty Quantification of PCB Lines

11:50
Til Hillebrecht, Tommy Weber, Johannes Alfert, Christian Schuster
Hamburg University of Technology, Germany
Unified Pre-Processing Steps Reducing the PCB Design Space to Enable ML Applications for Signal and Power Integrity Analysis

12:10
Ahsan Javaid, Ramachandra Achar
Carleton University, Canada
Efficient Multiconductor Transmission Line Analysis via Hybrid Deep Equilibrium NN Model

14:00 – 14:40 **KEYNOTE**

Giovanni Frattini
Analog Devices, Italy
What Does It Take to Make an Isolated Power Converter as a System-In-Package: an IC Designer's Perspective

SESSION 2
14:40 – 15:40 **DESIGN OPTIMIZATION**
Chair: Paolo Manfredi

14:40
Jordan R. Keuseman, Timothy Daun-Lindberg, Chad M. Smutzer, Clifton R. Haider
Mayo Clinic, USA
Tuning Unconventional Control Parameters for Optimal Transient Load Response in Multiphase Constant On-Time Switching Converters

15:00
Yens Lindemans, Thijs Ullrick, Ivo Couckuyt, Dirk Deschrijver, Tom Dhaene
Ghent University – imec, Belgium
Bayesian Optimization of Microwave Filters: A Physics-Informed Approach Using the Szegö Kernel

15:20
Abdullah Kayacan (1), Mustafa Gökçe Baydoğan (1), Ahmet Cemal Durgun (2), Kemal Aygün (3), Duye Ye (3), Cemil Geyik (3), Tolga Memioğlu (3)
(1) Boğaziçi University, Türkiye; (2) Middle East Technical University, Türkiye; (3) Intel Corporation, USA
Shadow Void Optimization of Microelectronic Packages with Tree-based Learners

15:40 – 15:50 **IEEE TC-EDMS**

Antonio Maffucci
University of Cassino and Southern Lazio, Italy
Activity of the IEEE Electrical Design, Modeling and Simulation technical committee

15:50 – 16:00 **SPONSOR PITCH**

STMicroelectronics, Italy
Rahul Kumar

16:00 – 16:40 **POSTER SESSION**

Chair: Tommaso Bradde

P-01

Sayed Mobin, Xu Wang, Harrison Pham, Pavan Gupta, Judy Crane

Alphabet Inc, USA

Navigating the Signal Seas: Addressing MIPI C-PHY Signal Integrity Challenges in a Typical Camera Module

P-02

Hung-Chun Kuo, Po-Chih Pan, Li-Chieh Hung, Ming-Fong Jhong, Chen-Chao Wang

Advanced Semiconductor Engineering, Taiwan

Worst Eye Performance Analysis for Advanced Package Die-to-Die Interconnects

P-03

Artur D. Pescador (1), Daniel N. de Araujo (2), Stefan J. de Araujo (3), Peter Mas (4)

(1) Université Paris-Dauphine-PSL, France; (2) Siemens, USA; (3) University of Texas Austin, USA; (4) Siemens, France

Current Density Prediction Using Neural Operators

P-04

Ethan Thieme (1,2), Biliana Paskaleva (1), Xu Chen (2), Pavel Bochev (1)

(1) Sandia National Laboratories, USA; (2) University of Illinois at Urbana-Champaign, USA

A Hammerstein Approach for Compact Model of Nonlinear Circuits with Arbitrary Terminations

P-05

Rıza Arman Tosun (1), Deniz Kuzucu (1), Ahmet Cemal Durgun (1), Mustafa Gökçe Baydoğan (2)

(1) Middle East Technical University, Türkiye; (2) Boğaziçi University, Türkiye

Fine-Pitch Interconnect Modeling Using Physics-Informed Neural Networks

P-06

Khitem Lahbacha (1), Antonio Maffucci (1), Giulia Di Capua (1), Gianfranco Miele (1), Andrea Gaetano Chiariello (2), Thi Dao Pham (3), Djamel Allal (3)

(1) University of Cassino and Southern Lazio, Italy; (2) University of Campania "Luigi Vanvitelli", Italy; (3) Laboratoire National de Métrologie et d'Essais, France

Signal Integrity Analysis and Measurement of Thin Film Microstrip Lines (TFMSLs)

P-07

Ifiok Umoh (1), Adrianna Hinojosa (1), Adefisayo Adepetun (1), Benjamin Lopez (2)

(1) Intel Corporation, USA; (2) Intel Corporation, Mexico

Analysis of BGA/Socket Differential Signal Pin-Field Egress For Improved Signaling Performance

P-08

Vipul Kumar Nishad (1), Atul Kumar Nishad (2)

(1) Indian Institute of Technology Ropar, India; (2) National Institute of Technology Warangal, India

Frequency-Dependent Mutual Inductance in Broadside-Coupled Superconducting Striplines

P-09

Glauber De Freitas Lima (1), Yve Lembeye (2), Fabien Ndagijimana (3), Jean-Christophe Crebier (2)

(1) CEA, LETI, DRT, Univ. Grenoble Alpes, France; (2) Univ. Grenoble Alpes, CNRS, Grenoble INP, France; (3) Univ. Grenoble Alpes, France

Near field radiated EMI signature characterization of modular power converters based on Dual Active Bridge: from calibration to results

May 13, Tuesday

09:00 – 10:20

SESSION 3

MACROMODELING

Chair: Ramachandra Achar

09:00

Stefan de Araujo (1), James Pingenot (2), Daniel de Araujo (2)

(1) University of Texas Austin, USA; (2) Siemens, USA

Acyclic Connected Graph Optimization for Generative Measurement Based Models

09:20

Bijan Shahriari, Roni Khazaka

McGill University, Canada

High Order Polynomial Projection Operators for Circuit Macro-Modeling

09:40

Antonio Carlucci (1), Ion Victor Gosea (2), Stefano Grivet-Talocia (1)

(1) Politecnico di Torino, Italy; (2) Max Planck Institute for Dynamics of Complex Technical Systems, Germany

An Extension of Vector Fitting to Weakly Nonlinear Circuits

10:00

Rahul Kumar (1), Manish Bansal (1), Anil Kumar Dwivedi (1), Kirtiman Singh Rathore (1), Rhani Menzer (2)

(1) STMicroelectronics Pvt Ltd, India; (2) STMicroelectronics Pvt Ltd, France

Bridging the Gap: Correlating IBIS-AMI Simulations with Post-Silicon Measurements for a 6.25 Gbps Transmitter

10:20 – 10:30 **SPONSOR PITCH**

Huawei, Italy
Marco De Stefano

10:30 – 10:40 **SPONSOR PITCH**

ESSS-Ansys, Italy
Andrea Serra

11:00 – 12:30 **INDUSTRY PANEL**
Chairs: Nicola Femia and Giulia Di Capua

11:00
Tiziano Morganti
EPC – Efficient Power Conversion, Italy
EPC GaN technology: exploiting the fastest power switch in the market

11:20
Fabio Quaglia
Analog Devices Inc., Italy
Driving and protecting GaN power switches: challenges and opportunities

11:40
Francesco Palomba
Keysight Technologies, Italy
How to add the effects of parasitics and return currents to your power converter simulations to get your circuit to work faster and more predictably

12:00
Open Discussion Panel

14:00 – 14:40 **KEYNOTE**

Andrea Ferrari
Cambridge Graphene Centre, University of Cambridge, UK
Graphene and Layered Materials for Photonics and Optoelectronics

SESSION 4
14:40 – 15:40 **HIGH SPEED CHANNELS**
Chair: Yutaka Uematsu

14:40
Seonghi Lee, Seongho Woo, Seunghun Ryu, Sanguk Lee, Hyunwoo Kim, Jinwook Lee, Dongkyun Kim, Jiseong Kim, Seungyoung Ahn
Korea Advanced Institute of Science and Technology, Republic of Korea
A Novel Termination Resistance-Controlled Passive Equalization Method for Signal Integrity Enhancement in High-Speed Channel

15:00
Nikhita Baladari (1), Trent Uehling (2), Frank Paglia (2), Stan Cejka (2)
(1) NXP Semiconductors, Netherlands; (2) NXP Semiconductors, USA
Design and Electrical Modeling of High-Speed Interfaces in a Novel Chiplet Package

15:20
Mekala Girish Kumar (1), Yash Agrawal (2), Rohit Sharma (3)
(1) VIT-AP University, India; (2) Dhirubhai Ambani Institute of Information and Communication Technology, India; (3) Indian Institute of Technology Ropar, India
High Frequency Analysis of Cu-CNT based Tapered TSV Bumps

SESSION 5
16:00 – 17:00 **MEASUREMENT BASED MODELS**
Chair: Grégory Houzet

16:00
Luigi Ferrigno (1), Vincenzo Mottola (1), Simone Palazzo (1), Annunziata Sanseverino (1), Alessandro Sardellitti (2), Antonello Tamburrino (1,3)
(1) University of Cassino and Southern Lazio, Italy; (2) Universitas Mercatorum, Italy; (3) Michigan State University, USA
Dimensional Analysis and FPGA-Based Implementation for Real-Time Thickness and Conductivity Estimation in Eddy Current Testing

16:20
Tommaso Bradde (1), Arne Schröder (2), Dierk Bormann (3), Alexandru Savca (2), Stefano Grivet-Talocia (1)
(1) Politecnico di Torino, Italy; (2) Hitachi Energy Research, Switzerland; (3) Hitachi Energy Research, Sweden
Measurement and Modeling of Bias-Dependent Powder Cores Permeability

16:40

Simone Negri (1), Xiaokang Liu (1), Giordano Spadacini (1), Sergio A. Pignari (1), Flavia Grassi (1), Damian Halicki (2), Aurora Sanna (2)
(1) Politecnico di Milano, Italy; (2) STMicroelectronics, Italy

Characterization of miniaturized transformers at varying operating power

May 14, Wednesday

SESSION 6

09:00 – 10:20 **PACKAGE DESIGN / POWER INTEGRITY**

Chair: Riccardo Trinchero

09:00

Jun-Bae Kim, Kwangho Kim, Chang Soo Yoon , Janghoo Kim, Jeongsik Hwang , Yoo-Chang Sung, Won-Joo Yun , Seung-Jun Bae
Samsung Electronics, South Korea

Simulation-Based Analysis of Land-Side Capacitor Integration in LPDDR5 DRAM

09:20

Marco Occhiali (1), Aurora Sanna (2), Simona Cucchi (2), Georgios Korompilis (3), Cristina Somma (2), Damian Halicki (2)
(1) Ansys, Italy; (2) STMicroelectronics, Italy; (3) Ansys, Greece

Power Integrity Performance Variation Induced by Degassing Holes in BGA Packages

09:40

Steve Sandler
PICOTEST, USA

Ultra-Low PDN Impedance Measurement Using Very Short Time Domain Acquisition

10:00

José E Schutt-Ainé (1), Patrick Goh (2), Yi Zhou (1)
(1) University of Illinois at Urbana Champaign, USA; (2) Universiti Sains Malaysia, Malaysia

Stability of VinC LIM in Power Distribution Network Analysis

SESSION 7

10:50 – 12:10 **CROSS TALK & NOISE REDUCTION / MEMRISTORS**

Chair: Jose Schutt-Aine

10:50

Yutaka Uematsu

Hitachi Ltd., Japan

Hybrid-type Power-over-data-line Filters for Mode Conversion Noise Reduction

11:10

Nicola Femia (1), Giulia Di Capua (2), Antonio Maffucci (2)

(1) University of Salerno, Italy; (2) University of Cassino and Southern Lazio, Italy

Power-to-Control Crosstalk in Power Electronic Circuits

11:30

Khitem Lahbacha (1), Antonio Maffucci (1), Andrea Gaetano Chiariello (2)

(1) University of Cassino and Southern Lazio, Italy; (2) University of Campania "L. Vanvitelli", Italy

Voltage-Drop Analysis of 1R-1D Memristor Crossbar Arrays

11:50

Suyash Kushwaha (1), Chintu Bhaskara Rao (1), Shamini P R (1), Sourajeet Roy (2), Rohit Sharma (1)

(1) Indian Institute of Technology Ropar, India; (2) Indian Institute of Technology Roorkee, India

Impact of Scaling on Large Crossbar Arrays for Neuromorphic Applications

12:10 – 12:30 **CLOSING SESSION**

14:00 – 18:00 **IBIS SUMMIT**

Chair: Markus Buecker

Program to be announced